

## DETAILED ACTION

### *Allowable Subject Matter*

1. Claims 3-5 and 8 are allowed.
2. The following is an examiner's statement of reasons for allowance:

As to claim 3, the prior art fails to disclose or suggest "an image processing device that reads an image signal from a solid-state image-pickup element where a plurality of unit pixels including a transistor for detecting a light signal and a photo diode are arranged in a matrix, the device comprising:

a first shift register connected to a line of the matrix for reading out an image signal, the first shift register selecting a line where a signal in response to carriers accumulated in an accumulation state for generating carriers in the photo diode in response to received light is read out;

a second shift register connected to a line for clearing an image signal, the second shift register selecting a line for clearing an image signal where residual carriers in the solid-state image-pickup element are discharged from the solid-state image-pickup element;

**a first output circuit that outputs a reset signal to the first shift register when a direction of scanning lines of the matrix is changed;**

a second output circuit that outputs shift data applied to a line for reading out an image signal, based on which a selection signal for selecting a line for reading out an

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image signal is output, to the first shift register, when a number of lines between the line for reading out an image signal and the line for clearing an image signal is equal to or less than a total number of lines in the matrix and a direction of the scanning lines of the matrix is changed,

wherein the second output circuit inhibits the output of the shift data, based on which the selection signal is output, to the first shift register, when the number of lines between the line for reading out an image signal and the line for clearing an image signal is more than the total number of lines in the matrix.

As to claim 5, similarly, the prior art fails to disclose or suggest “an image processing device that reads an image signal from a solid-state image-pickup element where a plurality of unit pixels including a transistor for detecting a light signal and a photo diode are arranged in a matrix, the device comprising:

a first shift register connected to a line of the matrix for reading out an image signal, the first shift register selecting a line where a signal in response to carriers accumulated in an accumulation state for generating carriers in the photo diode in response to received light is read out;

a second shift register connected to a line for clearing an image signal, the second shift register selecting a line for clearing an image signal where residual carriers in the solid-state image-pickup element are discharged from the solid-state image-pickup element;

**a first output circuit that outputs a reset signal to the first shift register  
when a direction of scanning lines of the matrix is changed;**

a second output circuit that outputs shift data applied to a line for reading out an image signal, based on which a selection signal for selecting a line for reading out an image signal is output, to the first shift register, when a number of lines between the line for reading out an image signal and the line for clearing an image signal is equal to or less than a total number of lines in the matrix and a direction of the scanning lines of the matrix is changed,

wherein the second output circuit outputs the selection signal when generating an interlacing frame according to frame rate.

Claims 4 and 8 are allowed as being dependent upon the allowed claims 3 and 5, respectively.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Inquiries***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHIA-WEI A. CHEN whose telephone number is

(571)270-1707. The examiner can normally be reached on Monday - Friday, 7:30 - 17:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, NgocYen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chia-Wei A Chen/  
Examiner, Art Unit 2622

*/Ngoc-Yen T. VU/  
Supervisory Patent Examiner, Art Unit 2622*